REMARKS

The Office Action dated November 4, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this Amendment, claims 2, 5, 12 15 and 17 have been cancelled. Claims 6 and 16 have been rewritten in independent form. Claims 1, 6-11, 14, 16, 18 and 20 have been amended to more clearly particularly point out and distinctly claim the invention. Claim 21 is newly added. No new matter has been added. Accordingly, claims 1, 4, 6-11, 14, 16, 18, 20 and 21 are pending in this application and are submitted for consideration.

Applicant acknowledges and thanks the Examiner for indicating that claims 4 and 14 are allowed over the prior art and that claims 6 and 16 would be allowable over the prior art if amended to be in independent form. By this Amendment, claims 6 and 16 have been written in independent form. Therefore, Applicant submits that these claims are also in condition for allowance.

Claims 11 and 14 were objected to for minor informalities. By this amendment, the claims have been amended as suggested by the Examiner. Therefore, it is requested that the objection be withdrawn.

Claims 1, 2, 5-11, 15, 16, 18 and 20 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. By this amendment claims 2, 5 and 15 have been cancelled and claims 6-11, 16, 18 and 20 have been further amended. Therefore, Applicant respectfully requests that the rejection be withdrawn.

Claims 1 and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zhou, et al. (U.S. Patent No. 6,362,669, "Zhou"). However, Applicant respectfully

submits that claims 1 and 10 recite subject matter that is neither disclosed nor suggested in the prior art.

Applicant's amended claim 1 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other. A main reset signal generator including a plurality of pulse generators is provided for respectively generating pulses on the basis of a translation edge for a corresponding one of said sub power-on reset signals. A composite circuit synthesizes the pulses to generate a main power on reset signal.

Applicant's amended claim 7 recites a method of initializing a semiconductor integrated circuit comprising the steps of: generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on; respectively generating pulses on the basis of a transition edge for a corresponding one of the sub power-on reset signals; and synthesizing the pulses to generate the power-on reset signal.

Zhou discloses a power-on reset circuit that delays de-assertion of a POR control signal in an IC device. When unstable power levels are detected, the POR control signal is maintained in an asserted condition until the IC device is fully reset. As shown in Fig. 5, POR circuit 500 includes a one-shot delay circuit 520 and a power-up delay circuit 530 connected in parallel between detection 120 and NOR gate 540. Inverter 550 is connected to the output terminal of NOR gate 540, and generates control signal POR. One-shot delay circuit 520 includes first inverter 522 is connected to an output terminal of detector circuit 120, detector circuit 120 generates detection signal POR1. A lock circuit 524 having a first input terminal connected to the output terminal of inverter

522, and a one-shot circuit 526 having an input terminal connected to the output terminal of lock circuit 524.

Power-up delay circuit 530 includes two or more series-connected inverters 532 and 534. Inverts 532 and 534 delay the transmission of high-to-low changes of detection signal POR1 for a longer delay period than low-to-high changes.

However, Zhou fails to disclose or suggest a main reset signal generator including a plurality of pulse generators, as recited in amended claims 1 and 7.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 1 and 7, is not anticipated within the meaning of 35 U.S.C. § 102, and request that the rejection be withdrawn.

Claims 1, 2, 7-12, 17 and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ikehashi et al. (U.S. Patent No. 6, 3, 51, 179, "Ikehashi") in making this rejection, the office action took the position that Ikehashi discloses all the elements of the claimed invention. By this amendment, Claims 2, 12 and 17 have been cancelled. The subject matter of claim 2 has been incorporated into Claim 1. Therefore, the rejection is moot with respect to these claims. However, the Applicant respectfully submits that claims 1, 7-11 and 20 recite subject matter neither disclosed nor suggested by the prior art.

Applicant's amended claim 8 recites a semiconductor integrated circuit having a plurality of sub reset signal generators, including transistors having threshold values, for generating a plurality of sub power-on reset signals on basis of the respective threshold values of each of the transistors, when detecting that a power supply is switched on. A main reset signal generator including a plurality of pulse generators is provided for

respectively generating pulses on the basis of a transition edge for a corresponding one rectangular pulse as a main power-on reset signal to initialize an internal circuit according to at least one of the sub power-on reset signals. A composite circuit synthesizes the pulses to generate a main power-on reset signal.

Applicant's amended claim 9 recites a semiconductor integrated circuit including a first sub reset signal generator, having a first transistor having a first threshold value when detecting that a power supply is switched on, for generating a first sub power-on reset signal on basis of the first threshold value. A second sub reset signal generator, including a second transistor having a second threshold value, is provided for generating a second sub power-on reset signal on basis of the second threshold value, when detecting that a power supply is switched on. A main reset signal generator including a plurality of pulse generators is provided for respectively generating pulses on the basis of a transition edge for a corresponding one of the first sub power-on reset signal and the second sub power-on reset signal. A composite circuit is provided for synthesizing the pulses to generate a main power-on reset signal.

Applicant's amended claim 10 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other when detecting that a power supply is switched on. A plurality of pulse generators generate pulses on the basis of the plurality of sub power-on reset signals, respectively, at least one of the pulses being a rectangular pulse. A composite circuit synthesizes the pulses to generate a main power-on reset signal.

Applicant's amended claim 11 recites a method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of: generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors when detecting that a power supply is switched on; respectively generating pulses on the basis of a transition edge for a corresponding one of the sub power-on reset signals, at least one of the pulses including a rectangular pulse; and synthesizing the pulses to generate the main of the power-on reset signal.

Applicant's amended claim 20 recites a method of initializing a semiconductor integrated circuit having a plurality of sub reset signal generators including transistors having threshold values, the method comprising the steps of: generating a plurality of sub power-on reset signals, each according to respective threshold values of each of the transistors when detecting that a power supply is switched on; respectively generating pulses on the basis of a transition edge for a corresponding one of the sub power-on reset signals, the pulses not overlapping each other when threshold values of transistors formed in the semiconductor integrated circuit are typical values; synthesizing the pulses to generate the main power-on reset signal.

Ikehasi discloses a semiconductor integrated circuit having a power supply circuit that prevents a malfunction caused by a transient change in power supply voltage. Ikehashi generates a pulse when the power supply is switched on and another when the power is switched off. However, contrary to this, in the present invention, a plurality of pulses are generated when the power supply is switched on, as recited in claims 1, 7-11 and 20.

Therefore, it is respectfully submitted that Applicant's invention, as set forth in claims 1, 7-11 and 20, is not anticipated within the meant of the 35 U.S. C § 102.

Claims 8, 9, 11, 18, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhou. In making this rejection, the Office Action took the position that Zhou discloses all the elements of the claimed invention, except for disclosing the generation of signals on the basis of respective threshold valued of the transistors.

However, as will be discussed below, Applicant submits that claims 8, 9, 11, 18 and 20 recite subject matter neither taught nor disclosed in any combination of the prior art.

Applicant's amended claim 18 recites a semiconductor integrated circuit including a plurality of sub reset signal generators for generating a plurality of sub power-on reset signals at timings different from each other, when detecting that a power supply is switched on. A main reset signal generator including a plurality of pulse generators is provided for respectively generating pulses on the basis of a transition edge for a corresponding one of the sub power-on reset signals. A composite circuit synthesizes the pulses to generate a main power-on reset signal. The main reset signal generator generates the main power-on reset signal having pulses respectively corresponding to each of the sub power-on reset signals, when threshold values of transistors formed in the semiconductor integrated circuit are typical values.

With respect to claim 8, the Office Action took the position that it would have been obvious to form each of the inverters as a CMOS inverter, and each of the logic devices using appropriate combinations of MOS transistors.

With respect to claim 9, the Office Action took the position that with respect to Fig. 6(f) of Zhou, the main reset signal generator 540, 550 generates pulse signal POR.

With respect to claim 11, the Office Action took the position that it would have been obvious to use CMOS inverters for each of the inverts of Zhou.

With respect to claim 18, the Office Action took the position that transistors are well-known means for forming inverters.

With respect to claim 20, the Office Action took the position that it would have been obvious to use transistors within the inverters of Zhou.

However, firstly, the Office Action has failed to provide motivation as to why one of ordinary skill in the art would be compelled to make the suggested modifications. Secondly, Zhou, in contrast to the Applicant's present invention, fails to disclose or suggest a main reset single generator including a plurality of pulse generators, as recited in amended claims 8, 9, 11, 18 and 20.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 8, 9, 11, 18 and 20, is not obvious within the meaning of 35 U.S.C. § 103.

Claims 5 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhou in view of Lee. In making this rejection, the Office Action took the position that Zhou discloses all the elements of the claimed invention. Lee is cited for curing the deficiencies of Zhou.

By this Amendment, Claims 5, and 15 have been cancelled and the subject matter incorporated into Claims 6 and 16. Therefore, the rejection is moot.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1, 7-11, 18 and 20, new claim 21 (claims 4

and 14 already being indicated as allowed and claim 6 and 16 being indicated as allowable) are currently pending in the above-identified U.S. patent application and the prompt issuance of a Notice of Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00025.**

Respectfully submitted,

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